REMARKS

Favorable reconsideration and allowance of the subject application are respectfully requested in view of the following remarks.

Summary of the Office Action

Claims 1-8, 13-16 and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Hayashi et al.* (U.S. Patent No. 6,133,092).

Claims 9-12, 14 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayashi et al.* in view of *Xing* (U.S. Patent No. 6,492,222).

Summary of the Response to the Office Action

Applicants have amended the abstract, the specification, and claims 1, 7, 8, 13, 15 and 32 by this amendment. In particular, the abstract, the specification, and claims 1, 8, 13, and 15 have been amended to correct a typographic error, i.e., replacing the symbol "Tu" with --Ru--. Support for these changes can be found, for example, at page 9, line 9 of the original specification.

In addition, claim 31 has been canceled without prejudice or disclaimer and claim 33 has been newly added. Accordingly, claims 1-30, 32 and 33 are currently pending with claims 17-30 directed to non-elected inventions.

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1-8, 13-16 and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by *Hayashi et al.* This rejection is respectfully traversed for at least the following reasons.

With regard to claim 31, Applicants respectfully request withdrawal of the rejection of claim 31 as the cancellation of claim 31 renders the rejection moot.

With regard to claims 1-8 and 13-16, Applicants respectfully submit that *Hayashi et al.* does not anticipate the present claimed invention because *Hayashi et al.* does not disclose all of the features of the claimed invention. For instance, it is respectfully submitted that *Hayashi et al.* fails to disclose at least the claimed combinations including a barrier layer "consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ ($0 < x < 1$), where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb," as set forth in independent claims 1, 8 and 13, and the claimed combination including "amorphous or microcrystal single layer expressed by an expression of $M1_xM2_{1-x}$ ($0 < x < 1$), where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb," as set forth in independent claim 15.

In contrast to the claimed invention as a whole, *Hayashi et al.* merely discloses a method of forming ferroelectric thin film layer (30), i.e., "a layer of layered superlattice material." Column 3, lines 44-45 and 59-50 of *Hayashi et al.* In the rejection, the Office Action appears to allege that the insulators (56) as taught by *Hayashi et al.*'s FIG. 4 include elements defined by formulas (6) and (7) in *Hayashi et al.*'s specification, such that *Hayashi et al.*'s insulators (56) correspond to the layer expressed by an expression of $M1_xM2_{1-x}$ ($0 < x < 1$) as recited in the claimed inventions. Specifically, the Office Action cites column 5, lines 29-47 of *Hayashi et al.* as teaching that the elements given by formulas (6) and (7) satisfy the express of $M1_xM2_{1-x}$ ($0 < x < 1$) as recited in Applicants' claimed combinations. However, *Hayashi et al.*'s insulator (56) does not include the elements given by formulas (6) and (7). In fact, *Hayashi et al.* teaches

'[i]nsulators, such as 56, separate the devices 71 [a transistor], 72 [a layered superlattice capacitor]." Column 5, lines 66-67.

In addition, *Hayashi et al.* teaches that the formulas (6) and (7) described in column 5 lines 25-47 pertain to a layer of layered superlattice material. More specifically, *Hayashi et al.*'s formula (6) is $(Sr_{1-w}M1_w)(Bi_{1-x}S_x)_2(\mathbf{Ta}_{1-y}\mathbf{M2}_y)_2O_9 + .\alpha M3O$, such that M2 may be **Nb**, Bi, or Sb (emphasis added), and *Hayashi et al.*'s formula (7) is $(1-z)Sr(Bi_{1-x}S_x)_2\mathbf{Ta_2}O_9+zABO_3 + \alpha MeO$ (emphasis added). Thus, neither *Hayashi et al.*'s formula (6) nor *Hayashi et al.*'s formula (7) teaches or suggests $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb, as set forth in Applicants' claimed combinations.

Hence, it is respectfully submitted that *Hayashi et al.* fails to teach or suggest at least the claimed combinations including a barrier layer "consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb," as set forth in independent claims 1, 8 and 13, and the claimed combination including "amorphous or microcrystal single layer expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb," as set forth in independent claim 15.

M.P.E.P. §2131 states "[t]o anticipate a claim, the reference must teach every element of the claim." Applicants respectfully submit that since *Hayashi et al.* does not teach or suggest all of the features of independent claims 1, 8, 13 and 15, *Hayashi et al.* does not anticipate claims 1, 8, 13, and 15. Further, since claims 2-7, 14 and 16 depend from claims 6 and 7, respectively, it

is respectfully submitted that *Hayashi et al.* also does not anticipate claims 9 and 10. Accordingly, withdrawal of this rejection of claims 6, 7, 9 and 10 under 35 U.S.C. §102(e) is respectfully requested.

Claim Rejection Under 35 U.S.C. §103(a)

Claims 9-12, 14 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayashi et al.* in view of *Xing*. This rejection is respectfully traversed.

Applicants respectfully submit that claims 9-12 and 14 are allowable at least because of their dependence upon claims 8 and 13 and for the reasons set forth above. In addition, Applicants respectfully submit that there does not exist motivation or suggestion in the prior art to combine *Hayashi et al.* in view of *Xing* to arrive at Applicants' claimed invention without impermissible hindsight. Accordingly, withdrawal of the rejection of claim 9-12 and 14 under 35 U.S.C. §103(a) is respectfully requested.

With regard to claim 32, to the extent that this rejection might be applied to the claim as newly-amended, it is respectfully traversed as follows. Applicants respectfully submit that the applied references, whether taken alone or in combination, do not teach or suggest at least the claimed combination including a barrier layer made of IrTaPt, as set forth in claim 32, as amended.

Specifically, Applicants respectfully submit that no portion of *Hayashi et al.*'s disclosure discusses using element Ir (Iridium) in a barrier layer or a barrier made of IrTaPt. Noting these deficiencies in *Hayashi et al.*, the Office Action cites *Xing* as allegedly teaching a Ir_xTa_{1-x} layer. Specifically, the Office Action cites column 9, lines 9-11 of *Xing* as teaching a IrTaPt layer. However, column 9, lines 7-11 of *Xing* describes:

> Preferably, the bottom electrode…is comprised of a noble metal or conductive oxide such as iridium, iridium oxide, Pt, Pd, PdOx, Au, Ru, RuOx, Rh, RhOx, LaSrCoO3, (Ba,Sr)RuO3, LaNiO3 or any stack of combination thereof.

Thus, Applicants respectfully submit that *Xing* does not discuss element Ta. Accordingly, Applicants respectfully traverse the Office Action's assertion that *Xing* teaches a Ir_xTa_{1-x} layer and request that evidence be provided in accordance with M.P.E.P. §2144.03.

Moreover, it is respectfully submitted that *Xing* is directed to a barrier layer consisting of Nitride base material, which is different from the present invention. Accordingly, Applicants respectfully submit that there does not exist motivation or suggestion in the prior art to combine *Hayashi et al.* in view of *Xing* to arrive at Applicants' claimed invention without impermissible hindsight.

M.P.E.P. §2143.03 instructs that "[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." Since, in view of the above, *Hayashi et al.* in view of *Xing* fails to teach or suggest each and every element set forth in independent claim 32, as amended, it is respectfully submitted that *Hayashi et al.* in view of *Xing* does not render claim 32 unpatentable. Accordingly, withdrawal of the rejection of claim 32 under 35 U.S.C. §103(a) is respectfully requested.

New Claim 33

Applicants have added new claim 33 to further define the invention. Applicants respectfully submits that claim 33 is allowable at least because of its dependence from claim 1.

Conclusion

In view of the foregoing, withdrawal of the rejections and allowance of the pending claims are earnestly solicited. Should there remain any questions or comments regarding this

response or the application in general, the Examiner is urged to contact the undersigned at the number listed below.

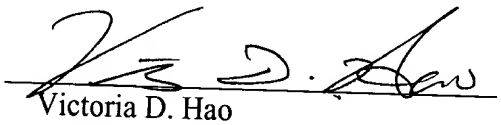
Attached hereto is a marked-up version of the changes made by the current amendment. The attachment is captioned "Version with markings to show changes made."

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

Dated: March 19, 2003

By: 
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

The abstract has been amended as follows.

The present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal expressed by the following expression:

$M1_xM2_{1-x}$

(0 < x < 1; M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

IN THE SPECIFICATION:

The paragraph beginning at page 3, line 13 has been amended as follows.

The first aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal expressed by the following expression: $M1_xM2_{1-x}$ (0 < x < 1;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 3, line 23 has been amended as follows.

Another aspect of the present invention is characterized by comprising: a lower electrode formed on a semiconductor substrate; a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and an upper electrode formed on said dielectric layer, wherein said lower electrode includes a barrier layer consisting

of amorphous or microcrystal expressed by the following: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 4, line 8 has been amended as follows.

Another aspect of the present invention is characterized by having: a lower electrode formed on a semiconductor substrate; a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and an upper electrode formed on said dielectric layer, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal between said dielectric layer and said upper electrode expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 4, line 19 has been amended as follows.

Another aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 5, line 1 has been amended as follows.

Another aspect of the present invention is characterized by including process forming an electrode formed on surface of a semiconductor substrate and process forming a dielectric film [an] on the upper layer thereof, wherein process forming said electrode includes process forming a barrier layer consisting of amorphous or microcrystal expressed by the following expression:

$M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 5, line 10 has been amended as follows.

Another aspect of the present invention is characterized by including: process forming a lower electrode on surface of a semiconductor substrate; process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode; and process forming an upper electrode on said dielectric layer, wherein said process forming the lower electrode includes process forming amorphous or microcrystal expressed by the following expression so as to form a dielectric capacitor: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 5, line 22 has been amended as follows.

Another aspect of the present invention is characterized by including: process forming a lower electrode on a semiconductor substrate; process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode; process forming a barrier layer consisting of amorphous or microcrystal expressed by the following expression on said dielectric layer: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb); and process forming an upper electrode on said barrier layer so as to form a dielectric capacitor.

The paragraph beginning at page 6, line 8 has been amended as follows.

Another aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 6, line 15 has been amended as follows.

A semiconductor device of the present invention includes a barrier layer consisting of amorphous or microcrystal between an electrode and a dielectric layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$;[)] M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The paragraph beginning at page 8, line 14 has been amended as follows.

A semiconductor device of the present invention is characterized by that having an electrode formed on a surface of a semiconductor substrate, wherein said electrode includes an amorphous [amorpous] or microcrystal barrier layer which includes at least an element chosen from a first group of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V and Cr and at least an element chosen from a second group of Ta, Ti, Zr, Hf, W, Y, Mo and Nb. A barrier effect is kept good with a ternary chemical compound or higher is used as a barrier. Matching grating constant becomes easier, making it possible to form an electrode with an excellent boundary characteristics.

The paragraph beginning at page 9, line 10 has been amended as follows.

Further, other than the above listed binary chemical compounds, a barrier layer of either amorphous or microcrystal of ternary chemical compounds or higher composed of at least an element from a first group of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V and Cr and at least an element from a second group of Ta, Ti, Zr, Hf, W, Y, Mo and Nb, such as IrTiPt for example, is applicable.

The paragraph beginning at page 25, line 10 has been amended as follows.

As described above, according to the present invention, a barrier layer consisting of amorphous or microcrystal is included as an electrode being expressed by the following expression:

$M1_xM2_{1-x}$ ($0 < x < 1$;

M1: Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, Cr;

M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

The barrier effect is large so as to prevent mutual diffusion of oxygen etc. and spike because the barrier layer consisting of the amorphous or microcrystal does not have clear grain boundary. Therefore, escape of oxygen from dielectric layer can be prevented so as to depress aging dielectric characteristic. Dielectric thin film formed on the amorphous or microcrystal is good in orientation performance so as to be possible to provide dielectric structure high in reliability.

IN THE CLAIMS:

Claim 31 has been canceled without prejudice or disclaimer.

Claims 1, 7, 8, 13, 15 and 32 have been amended as follows.

1. (Amended) A semiconductor device having an electrode formed on a surface of a semiconductor substrate, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

7. (Amended) A semiconductor device according to [any one of Claims 1 to 5] Claim 6, wherein said dielectric layer is PZT.

8. (Amended) A semiconductor device comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric layer formed on said lower electrode and constructed by a ferroelectric or dielectric having high dielectric constant; and

an upper electrode formed on said dielectric layer,

wherein said lower electrode includes a barrier layer consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

13. (Amended) A semiconductor device comprising:

a lower electrode formed on a semiconductor substrate;

a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having a high dielectric constant; [and]

an upper electrode formed on said dielectric layer; and[,]

[wherein said electrode includes] a barrier layer formed between said dielectric layer and said upper electrode, [a barrier layer] consisting of amorphous or microcrystal expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

15. (Amended) A semiconductor device having

an electrode formed on a surface of a semiconductor substrate,

wherein said electrode is constructed by amorphous or microcrystal single layer expressed by an expression of $M1_xM2_{1-x}$ $(0 < x < 1)$, where M1 is selected from a group consisting of Au, Pt, Ir, Pd, Os, Re, Rh, [Tu] Ru, Cu, Co, Fe, Ni, V, and Cr, and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W, Y, Mo, and Nb.

32. (Amended) A semiconductor device having

an electrode formed on a surface of a semiconductor substrate,

wherein said electrode includes an amorphous or microcrystal barrier layer [A semiconductor device according to claim 31, wherein said barrier layer is] made of IrTaPt.